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Full-Bridge T-type Isolated DC/DC Converter with Wide Input Voltage Range

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***Abstract*— The advent of the silicon carbide (SiC) power device with high voltage stress would simplify the power converter's circuit structure for high voltage applications since two-level topologies would be possible to instead three-level (TL) based topologies. This paper proposes a full-bridge (FB) T-type isolated DC/DC converter composed of four main power switches with high voltage stress (SiC MOSFET) and four auxiliary power switches with low voltage stress (Si MOSFET). Therefore, comparing with the conventional diode-clamped FB TL isolated DC/DC converter, the proposed converter has fewer circuit components and simpler circuit structure. What is more, a corresponding control strategy is proposed, which can not only realize zero-voltage switching (ZVS) but also achieve wide input voltage range. Finally, simulation and experimental results are both presented for verification.**

Keywords*— DC/DC converter, Full-bridge (FB), T-type, Wide input voltage range.

I. INTRODUCTION

Although AC distribution system is most widely used distribution system nowadays [1], [2], DC distribution system is a promising solution for the future power distribution system [3], [4] because the increasing applications of EV infrastructure, and renewable energy. The DC/DC converters are responsible for controlling power flow and converting the voltage level in the DC distribution system, so the research about the efficient and reliable DC/DC converters becomes a hot topic [5] - [7]. The three-level (TL) DC/DC converters become attractive because they can withstand the high input voltage and thus reduce the transmission loss. Many studies have been done on the TL isolated DC/DC converters in topics of extending soft switching range [8], [9], balancing voltages on the input capacitors [10], [11], reducing circulating currents [12], [13], minimizing and balancing currents on the input capacitors [14], and balancing currents among power switches [15].

T-type converter is another type of TL converter, which has been widely applied for inverters [16]. References [17] - [19] discussed about the T-type isolated DC/DC converters recently. Comparing with the conventional diode-clamped TL DC/DC converter, T-type converter has fewer circuit components and simpler circuit structure. The T-type DC/DC converters discussed in [17] - [19] belong to the half-bridge (HB) structure, thus they would be unsuitable for high power applications since the power switches' current stress on in HB structure is twice of that in FB structure. In addition, a major drawback of the T-type converter is that the main power switches' voltage stress is full input voltage. Fortunately, the advent of SiC power device would result in that the T-type DC/DC converter with SiC power device is possible for the high voltage applications because SiC power device's drain-source breakdown voltage is much higher than Si power device's.

In this paper, a FB T-type isolated DC/DC converter with SiC device is proposed for high-power and high-voltage applications. There are four main power switches with high voltage stress (SiC MOSFET) and four auxiliary power switches with low voltage stress (Si MOSFET) in the proposed converter. What is more, a control strategy composed of two modes is proposed, which not only can realize zero-voltage switching (ZVS) for main and auxiliary power switches but also can fulfill wide input voltage range. Finally, both simulation and experimental results are demonstrated for verification.

II. CIRCUIT STRUCTURE

Fig. 1 presents the proposed converter's circuit structure. In Fig. 1, C_1, C_2 are two input capacitors; V_1, V_2 are two voltages split by C_1, C_2 from input voltage V_{in}; S_1 - S_4 are four main power switches; S_5 - S_8 are four auxiliary power switches; D_1 - D_8 are body diodes of S_1 - S_8; C_{s1} - C_{s8} are parasitic capacitors of S_1 - S_8; T_r is an isolated transformer; L_r is the inductance of series inductor plus leakage inductance of T_r; D_{r1} - D_{r4} are four rectifier diodes; L_o is an output filter inductor; and C_o is an output filter capacitor.

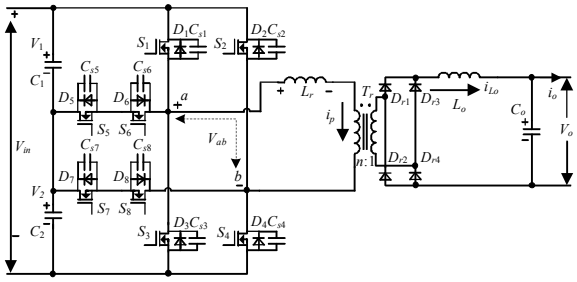


Fig. 1. Proposed converter's circuit structure.

In Fig.1, the input voltage is V_{in}; the voltage between point a and b is V_{ab}; the primary current of T_r is i_p; the current on L_o is i_{Lo}; the output voltage is V_o; the output current is i_o; the turns ratio of T_r is n. Table I shows the comparison results about the primary component number

between the conventional diode-clamped FB TL isolated DC/DC converter and proposed converter.

TABLE I.
COMPARISON RESULTS ABOUT PRIMARY COMPONENT NUMBER

Component number	Diode-clamped FB TL DC/DC converter	Proposed FB T-type DC/DC converter
Power switch	**8**	**8**
Clamping diode	**4**	**0**
Flying capacitor	**2**	**0**
Input capacitor	**2**	**2**

III. OPERATION PRINCIPLE

A ZVS control strategy with two working modes is proposed. Figs. 2(a) and 2(b) show main waveforms of mode I and II respectively, in which d_{rv1} - d_{rv8} are driving signals for power switches S_1 - S_8; T_s is one switching period; d_1, d_2 are duty ratios in T_s and are used for operation mode I and II respectively; d_{loss_I} and d_{loss_II} are duty ratio losses in T_s under the operation mode I and II respectively.

Mode I and II are applied for low and high input voltage respectively, which can thus achieve the wide input voltage range. As presented in Fig. 2, V_o is controlled by adjusting d_1, d_2 under mode I and mode II respectively.

Figs. 3 and 4 present operation circuits for explaining the working operations under mode I and II more clearly.

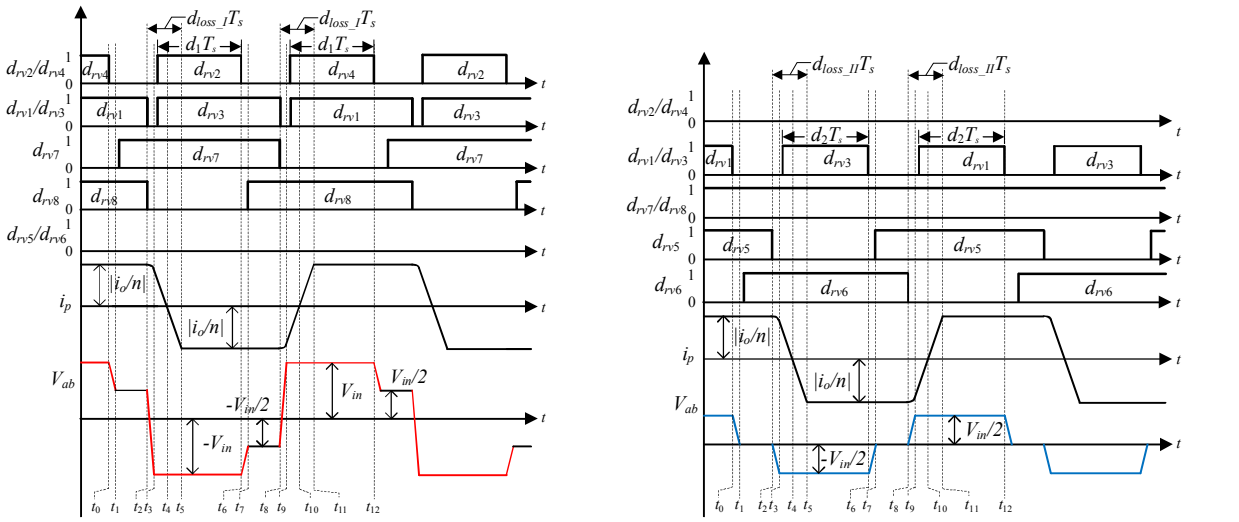
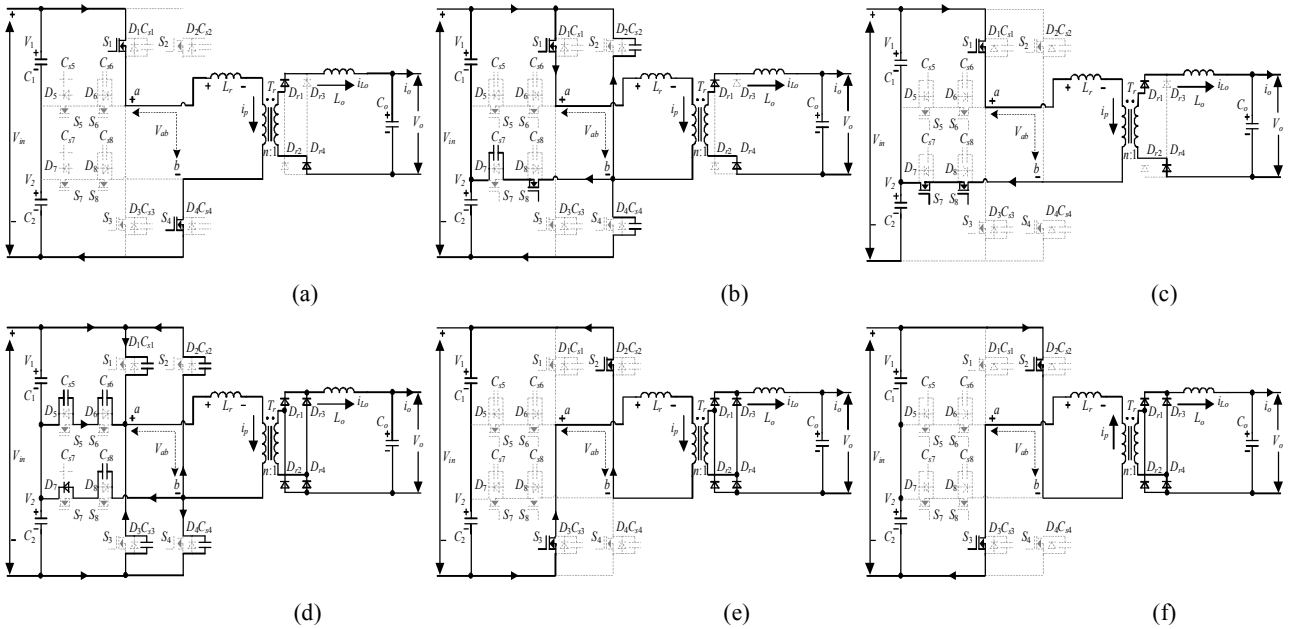
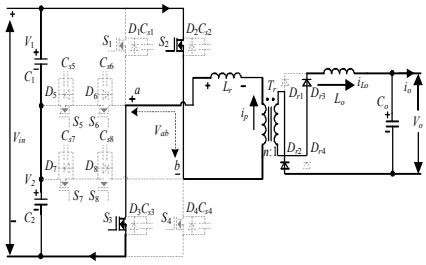


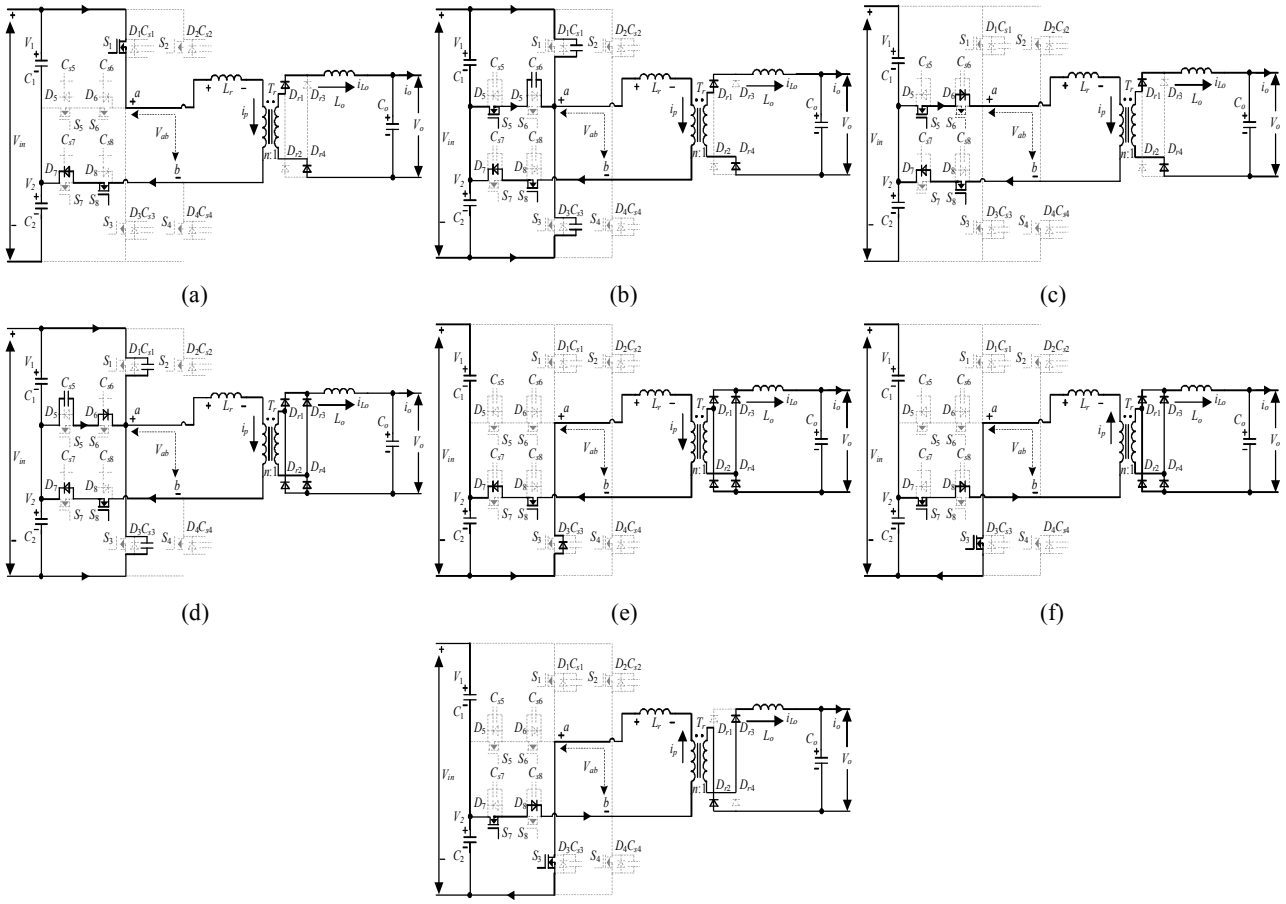
Fig. 2. Proposed control strategy. (a) Mode I. (b) Mode II.





(g)

Fig. 3. Operation circuits under mode I. (a) [before t_0] (b) [t_0-t_1]. (c) [t_1-t_2]. (d) [t_2-t_3]. (e) [t_3-t_4]. (f) [t_4-t_5]. (g) [t_5-t_6].



(a) (b) (c)

(d) (e) (f)

(g)

Fig. 4. Operation circuits under mode II. (a) [before t_0] (b) [t_0-t_1]. (c) [t_1-t_2]. (d) [t_2-t_3]. (e) [t_3-t_4]. (f) [t_4-t_5]. (g) [t_5-t_6].

IV. Analysis of Characteristic and Performance

A. Power Switches' Voltage Stresses

In steady working operations, the voltage stress on main power switches S_1 - S_4 are the input voltage (V_{in}), and the voltage stress on auxiliary power switches S_5 - S_8 are half of the input voltage (V_{in}/2).

B. Output Gain

Under mode I and II, the duty ratio losses named d_{loss_I} and d_{loss_II} can be calculated by (1) and (2) respectively.

$$d_{loss\_I} = \frac{2 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \tag{1}$$

$$d_{loss\_II} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \tag{2}$$

Under mode I, the average output voltage V_{o_I} can be obtained by (3).

$$V_{o\_I} = \frac{V_{in}}{n} \cdot (0.5 + d_1 - 2 \cdot d_{loss\_I}) = \frac{V_{in}}{n} \cdot (0.5 + d_1 - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}) \tag{3}$$

Under mode II, the average output voltage V_{o_II} can be obtained by (4).

$$V_{o\_II} = \frac{V_{in}}{n} \cdot (d_2 - d_{loss\_II}) = \frac{V_{in}}{n} \cdot (d_2 - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}) \tag{4}$$

The average output voltage $V_{o\_two\_level}$ in the basic FB two-level isolated DC/DC converter utilizing phase-shift control [20] can be calculated by (5).

$$V_{o\_two\_level} = \frac{V_{in}}{n} \cdot (2 \cdot d_{two\_level} - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}) \quad (5)$$

in which d_{two_level} is the overlap time between the leading and lagging power switch divided by one switching period.

Based on equations (3) - (5) and assuming that the basic FB two-level isolated DC/DC converter and proposed converter have the same circuit parameters (n=25:8 L_r=47.7uH, f_s=50kHz) and secondary circuits, theoretical relations between duty ratio and input voltage in proposed converter and FB two-level isolated DC/DC converter are presented in Fig. 5 under working conditions that V_o is 50 V and output power named P_o is 1 kW.

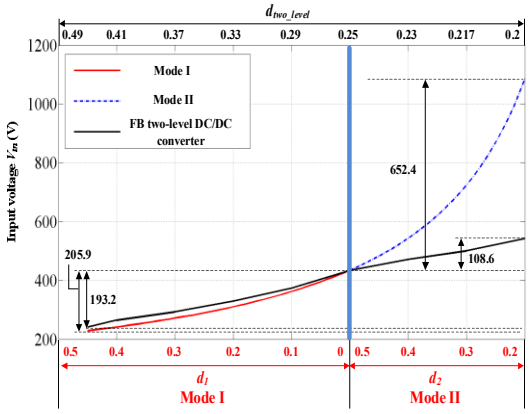


Fig. 5. Theoretical relation curves between the input voltage and duty ratio (V_o = 50 V, P_o = 1 kW, f_s = 50 KHz).

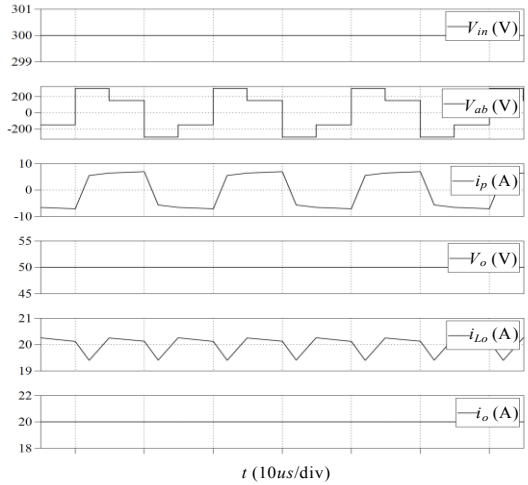
Note: Bottom X axis marked by red color represents the duty ratios in proposed converter; and top X axis represents the duty ratio in FB two-level isolated DC/DC converter.

V. Simulation and Experimental Verification

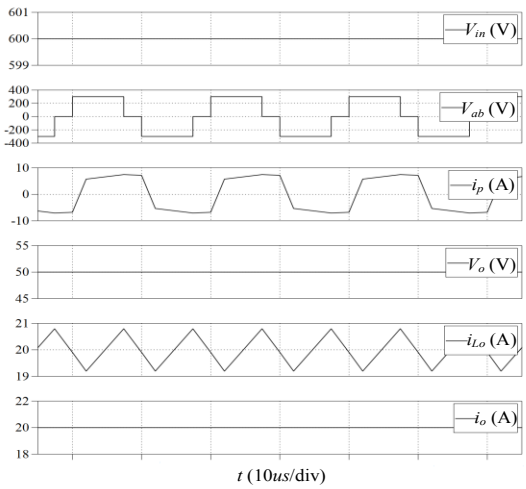
A. Simulation Verification

For verification, a simulation model is built in PLECS. The built simulation model's circuit parameters are presented in Table II.

Fig. 6 presents simulations results about V_{in}, V_{ab}, V_o, i_{Lo}, i_p, and i_o under mode I and II.



(a)



(b)

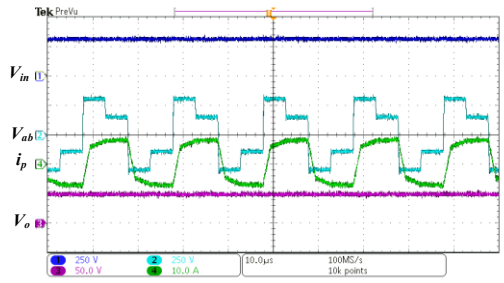
Fig. 6. Simulation results (V_o = 50 V, P_o = 1 kW). (a) V_{in} = 300 V (Mode I). (b) V_{in} = 600 V (Mode II).

Based on simulation results in Fig. 6, it can be obtained: 1) Mode I is applied when V_{in} is low (300 V) as presented in Fig. 6(a); 2) Mode II is applied when V_{in} is high (600 V) as presented in Fig. 6(b); and 3) the ripple current (i_{Lo}) on L_o under mode I is smaller than that under mode II.

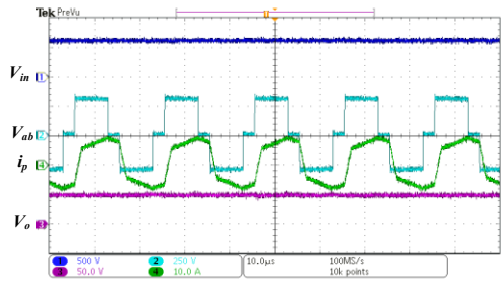
B. Experimental Verification

A 1 kW laboratory prototype is established for verification. The established proposed converter's circuit parameters are presented in Table II.

Fig. 7 presents the experimental results about V_{in}, V_{ab}, V_o, and i_p.



(a)



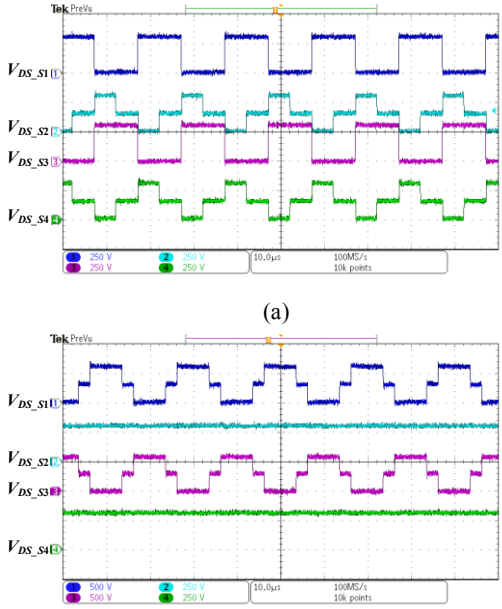
(b)

Fig. 7. Experimental results about V_{in}, V_{ab}, V_o, i_p (V_o = 50 V, P_o = 1 kW). (a) V_{in} = 300 V (Mode I). (b) V_{in} = 600 V (Mode II).

In Fig. 7, it can be seen: 1) Mode I is applied for the low voltage (V_{in} = 300 V) as presented in Fig. 7 (a); and 2) Mode II is applied for the high voltage (V_{in} = 600 V)

as presented in Fig. 7 (a).

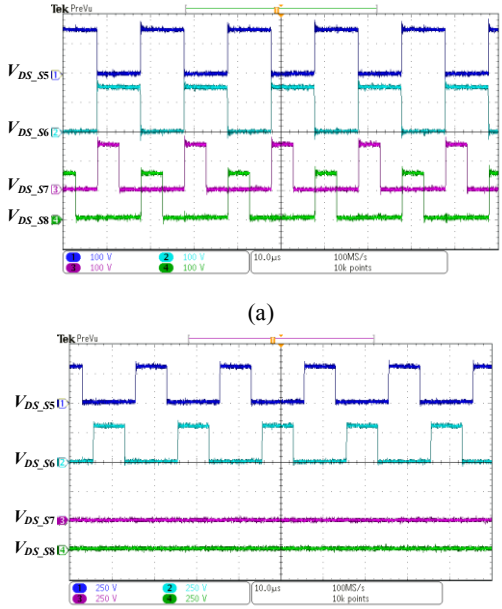
Figs. 8 and 9 present the power switches' drain-source voltage. In Figs. 8 and 9, V_{DS_S1} - V_{DS_S8} are drain-source voltages on S_1 - S_8. Based on experimental results in Figs. 8 and 9, it can be obtained: 1) main power switches' voltage stresses are about input voltage; and 2) auxiliary power switches' voltage stresses are about half of input voltage.



(a)

(b)

Fig. 8. Experimental results about V_{DS_S1} - V_{DS_S4} (V_o = 50 V, P_o = 1 kW). (a) V_{in} = 300 V (Mode I). (b) V_{in} = 600 V (Mode II).



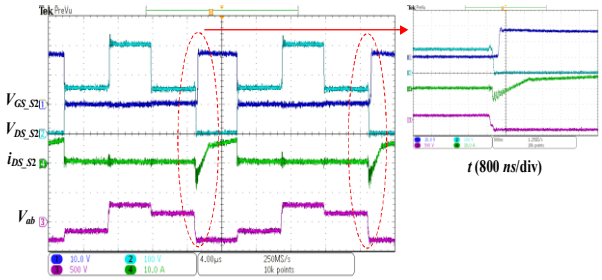
(a)

(b)

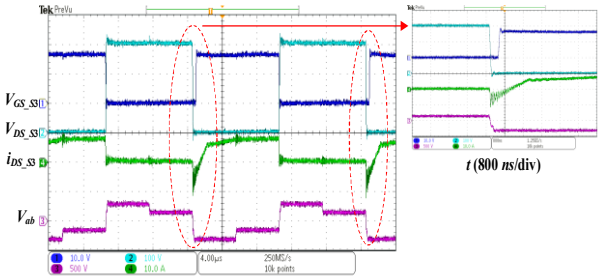
Fig. 9. Experimental results about V_{DS_S5} - V_{DS_S8} (V_o = 50 V, P_o = 1 kW). (a) V_{in} = 300 V (Mode I). (b) V_{in} = 600 V (Mode II).

Fig. 10 presents ZVS performances about S_2, S_3, S_7 under mode I when V_o is 50 V, V_{in} is 300 V, P_o is 1 kW. Fig. 11 shows ZVS performances of S_3 and S_6 under mode II when V_o is 50 V, V_{in} is 600 V, P_o is 1 kW.

Based on experimental results in Figs. 10 - 11, the followings can be obtained: 1) under mode I, main power switches S_2, S_3 and auxiliary power switch S_7 realize ZVS when P_o is 1 kW respectively; and 2) under mode II, the main power switch S_3 and auxiliary power switch S_6 realize ZVS when P_o is 1 kW. The other main power switches' and auxiliary power switches' ZVS performances under mode I and II are similar to that of 1) and 2).



(a)



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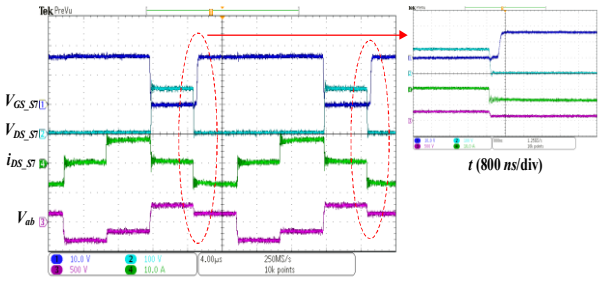
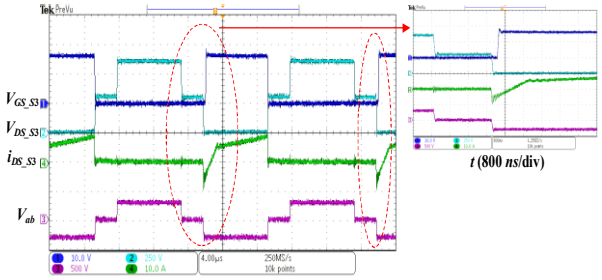
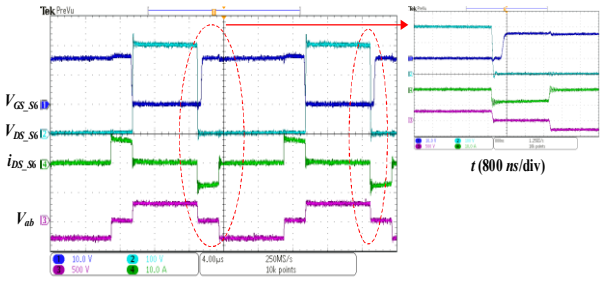


(c)

Fig. 10. ZVS performances (V_{in} = 300 V, V_o = 50 V, P_o = 1 kW Mode I). (a) S_2. (b) S_3. (c) S_7.



(a)



(b)

Fig. 11. ZVS performances (V_{in} = 600 V, V_o = 50 V, P_o = 1 kW Mode II). (a) S_3. (b) S_6.

VI. Conclusion

A FB T-type isolated DC/DC converter and corresponding control strategy is proposed in this paper. The proposed converter compromises four main power switches with the voltage stress of input voltage (SiC MOSFET) and four auxiliary power switches with the voltage stress of half of input voltage (Si MOSFET). Therefore, it has fewer circuit components and more compact circuit structure when comparing with the diode-clamped FB TL isolated DC/DC converter. What is more, the proposed control strategy not only can realize ZVS but also can fulfill wide input voltage range. Finally, both simulation and experimental results verify the proposed converter with its corresponding control strategy.

Appendix

TABLE II
Parameters of Simulation Model and Experimental Prototype

Main Power Switches S_1 - S_4	C3M0065090D
Auxiliary Power Switches S_5 - S_8	SPW47N60C3
Rectifier Diodes D_{r1} - D_{r4}	MBR40250TG
Turns Ratio of Transformer T_r (n : 1)	25 : 8
Inductance of Series Inductor plus Leakage Inductance L_r (uH)	47.7
Input Capacitors C_1 and C_2 (uF)	470
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (uH)	140
Switching Frequency (kHz)	50

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